MODELING OF THE FEED-THROUGH WIDEBAND (DC to 12.4 GHz) SAMPLING-HEAD

Sedki M. Riad
Electrical Engineering Dept.
Florida Technological University
Orlando, Florida 32816

and

Norris S. Nahman
Electromagnetics Division
National Bureau of Standards
Boulder, Colorado 80302

ABSTRACT

A model is developed from dimensional and electrical measurements in conjunction with electromagnetic and electronic theory. Calculations based on the model predict step response transition durations of 27.5 to 30.5 ps for gate bias values of -1.76 to -1.63 volts.

I. Introduction

Due to sampling-head bandwidth limitations, a time domain waveform observed by a sampling oscilloscope is not an exact duplicate of the signal waveform at the input terminal of the oscilloscope. The observed waveform is the convolution of the signal waveform with that of the oscilloscope's impulse response. In the frequency domain, the observed bandwidth (complex spectrum) is determined by the product of the complex signal spectrum and the complex transfer function of the oscilloscope. In order to determine the true signal waveform (and its complex spectrum), it is necessary to determine a model for the transfer properties of the oscilloscope.

The sampling oscilloscope considered here is used for observing signals from DC out to 12.4 GHz and transients with transition durations greater than about 30 ps. The one kind of sampling-head that is most commonly used in time domain reflectometry measurements is the feed-through sampling-head because of the convenience of usage in observing incident and reflected time domain signals on the same line.

In the present paper, the modeling method is applied to a typical feed-through sampling-head. The resultant physically based model is used to predict the oscilloscope's time domain response (and frequency domain response, if desired). The specific sampling-head to be considered here has a nominal band-width of 12.4 GHz and a nominal 28 picosecond (10% to 90%) transition duration (rise time). Previous work reported in the literature was based upon mainly mathematical models which considered in a limited way the physical structural and network properties of the sampling-head.[1] The modeling principles demonstrated here are readily adaptable to other sampling-heads.

II. Sampling-Head Construction

Figure 1 shows the balanced two diode feed-through sampling circuit and its physical structure (not-to-scale).[2,3] In the figure is is seen that the feed-through transmission line is tapered or stepped-down on both the input and output sides of the sampling gate; this is successively done through a three section compensated stepped-taper maintaining a 50 ohm impedance along the line. The sampling diodes are placed transverse to the axis of the transmission line, touching the inner conductor from both sides. In this region the inner conductor is a thin curved piece of metal that joins the two tapered sections together. The outer conductor forms a biconical cavity, which acts as a shorted biconical transmission line and as such shapes the strobe pulse. The biconical cavity is dielectric filled to mask the packaging capacitance of the sampling diodes to lessen the effect of the diodes on the 50 ohm characteristic impedance throughout the cavity.

III. Modeling of the Physical Structure

Precise measurements were performed on the physical dimensions of the disassembled sampling-head.[3] The result of this measurement together with the results of some TDR measurements on the biconical cavity, as will be described later, were used in forming an equivalent network (a model) for the sampling-head.

In modeling the feed-through transmission line, each of the step line discontinuities was modeled by an equivalent capacitor.[4,5] TDR measurement performed on the cavity with and without dielectric filling showed that:

a - the feed-through line in the cavity region is within ± 1 Ω from the 50 Ω characteristic impedance,
b - there is an inductive effect in the central portion of the cavity due to the metallic curved strip that connects the tips of the two inner conductor tapered sections, and
c - the dielectric constant of the dielectric filling the cavity is 2.21, which yields 22.2 ps for the biconical cavity travel time τ_{bc} (one way).

IV. Sampling Diodes

The sampling diodes that are used in the feed-through sampler are hot carrier (Schottky) type; the electrical model of such diodes is shown in Figure 2.[7,8,9] Static measurements were performed on the diodes to evaluate static characteristics. A set of TDR measurements were performed on the sampling-head once with both sampling diodes, another time with one of the diodes removed, and a third time with one open diode (acting as a packaging capacitance) to evaluate the diode's lead inductance and packaging capacitance. Another set of TDR measurements at various values for the diode's bias was needed to evaluate the voltage dependent junction capacitance of the diode.

V. The Sampling Pulse

The sampling pulse is formed in the biconical cavity by waveshaping a step-like strobe pulse transmitted to the cavity by a miniature coaxial line (wire line), Figure 1. A wideband sampling oscilloscope was used to observe this step-like strobe $v_{st}(t)$ at its entry to the wire line. The observed strobe was corrected to account for the measuring oscilloscope transition duration and impedance mismatches at both ends of the wire line. The distortion of the strobe pulse by the miniature transmission line was determined to be negligible using response data in [10].

VI. Computation of the Sampling-Head Step Response

The results of sections II through V above were combined with a sample storage feedback loop to form a complete model for the sampling-head. The total model was found to be too large to be handled by a large

CH1355-7/78/0000-0267$00.75

computer; accordingly, the model (network) was divided into two independent networks, in which case the step response could then be obtained by two separate calculations. The two networks are shown in Figures 2 and 3. The structure network in Figure 2 was used in the first calculation with the applied voltage step at the input-port, node 1,

$$v(t) = u(t) = 0 \ , \ t < 0$$
$$= V \ , \ t > 0.$$

The resultant quantity in the first calculation is the voltage at node 8, $v_8(t)$, which is called the structure step response, Figure 4. In the second, and final, calculation, the voltage waveform of node 8 was applied together with the strobe pule $v_{st}(t)$ to the network of Figure 3. The result of this second calculation is the sampled-data voltage given by the difference between the voltage drops across the sampling (storage) capacitors C_{s1} and C_{s2}. This difference represents the sampling-head output at a discrete time due to the applied step at the input port.

VII. Effect of Diode Bias on Sampling-Head Step Response

When the sampling process is scanned over the structure response function, the step response of the sampling-head is obtained. For a reverse bias of 1.63 volts applied to the diode sampling gate, the calculated step response 10% to 90% transition duration (rise time) was 30.5 ps while 1.76 volts produced a calculated transition duration of 27.5 ps, Figure 5.

The two bias values were obtained from experimental data. Using a given tunnel diode generator, experiments showed that the displayed waveform transition duration varied with gate bias, V_b, Figure 6. At 100% sampling efficiency (V_b = -1.63 volts) the measured transition duration was 33.7 + 2 ps. The minimum transition duration of 32.4 ± 2 ps was observed for a bias of -1.76 volts.

VIII. Analysis of Results

If the model for the sampling-head is accurate, then deconvolution (using the model) of either of the two observed waveforms (in VII) should yield the tunnel diode transition waveform; i.e., deconvolution of both observed waveforms should yield an identical result. To date, this has not been done for two reasons: (1) the experimental data was acquired from photographs giving uncertainties of measurement greater than + 2 ps and (2) the development of a suitable deconvolution routine has not been completed. However, the experiments are to be repeated using the NBS APMS [11] to acquire the data with a relative uncertainty of + 0.1 ps and to implement the deconvolution routine[12]. At present, an estimate of the data consistency can be made using the root-sum of the squares of the transition durations.

$$\tau_r = \left[\tau_s^2 + \tau_g^2 \right]^{1/2},$$

where τ_r, τ_s, and τ_g are the transition durations for the observed waveform, the sampling-head calculated response, and the tunnel diode transition waveform, respectively. Using ± 2 ps uncertainty about the observed transition duration, the estimated range of values for the tunnel diode transition duration is (a) 1.63 V bias, 8.6 to 18.6 ps and (b) -1.76 V bias, 12.9 to 20.7 ps. Hence, it can be concluded that the results are at least consistent in that the range of transition durations overlap. This does not preclude the possibility of obtaining two different deconvolution results in future studies which, in turn, would require further refinement of the model.

References

[1] D. Howard, A. Best and J. Umphrey, "The Wide-Band Sampling Gate: An Analysis, Characterization and Application Discussion," WESCON Tech. Papers, Pt. 6, Session 23, Paper 1, 1966.

[2] W. M. Grove, "Sampling for Oscilloscopes and Other RF Systems: DC Through X-Band," IEEE Trans. Microwave Theory & Techniques, Vol. MTT-14, pp. 629-635, December 1966.

[3] S. M. Riad, "The Theory and Application of the Homomorphic Transformation to Time Domain Spectroscopy and Scattering Problems," Ph.D. Dissertation, University of Toledo, Toledo, OH 1976, Ch. VI.

[4] J. R. Whinnery, H. W. Jamieson and T. E. Robbins, "Coaxial Lines Discontinuities," Proc. IRE, Vol. 32, pp. 695-709, November 1944.

[5] J. R. Whinnery and H. W. Jamieson, "Equivalent Circuits for Discontinuities in Transmission Lines," Proc. IRE, Vol. 32, pp 98-115, Feb. 1944.

[6] S. Ramo, J. R. Whinnery, and T. VanDuser, Fields and Waves in Communication Electronics, New York, N.Y.: J. Wiley, 1965, pp.462-465.

[7] J. N. Kaposhilin, "Hot Carrier Diode Opens New Vistas," Electronic Design, pp. 178-184, Mar. 1966.

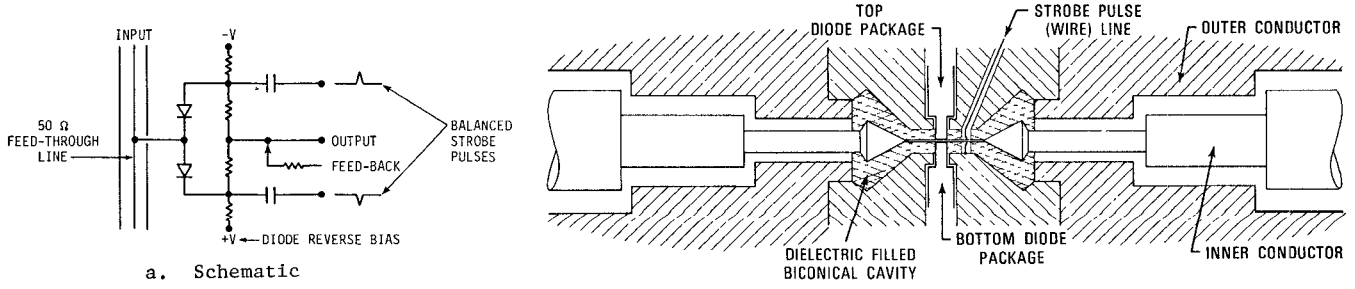
[8] Hewlett Packard Associates, "The Hot Carrier Diode Theory, Design, and Application," Application Note, AN 907, Hewlett Packard Co., Pala Alto, CA.

[9] R. J. Chaffin, Microwave Semiconductor Devices, New York, N.Y.: J. Wiley, 1973, Ch. 6.

[10] D. R. Holt and N. S. Nahman, "Coaxial-Line Pulse Response Error Due to a Planar Skin-Effect Approximation," IEEE Trans, Instru. & Meas., Vol. IM-21, No. 4, November 1972, pp 515-519.

[11] W. L. Gans, "Present Capabilities of the NBS Automatic Pulse Measurement System," IEEE Trans. Instru. & Meas., Vol. IM-25, No. 4, December 1976, pp. 384-388.

[12] Personal Communication on Deconvolution Routine Development, W. L. Gans, National Bureau of Standards, 276.04, Boulder, CO 80302.



a. Schematic

b. Constructional Detail

Figure 1. Balanced Diode Sampling Gate.

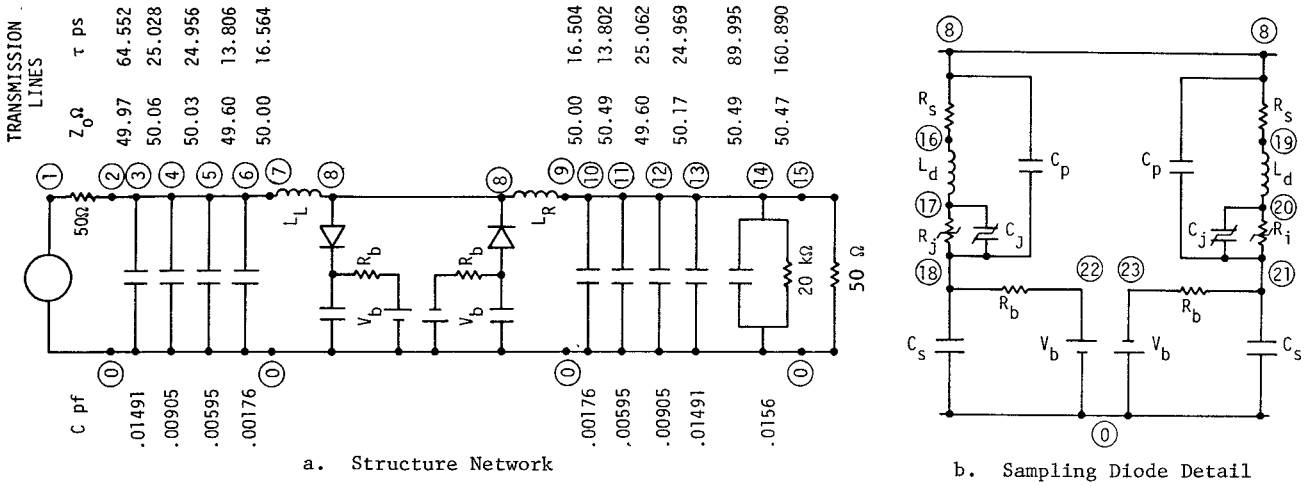


Figure 2. Sampling-Head Structure Network

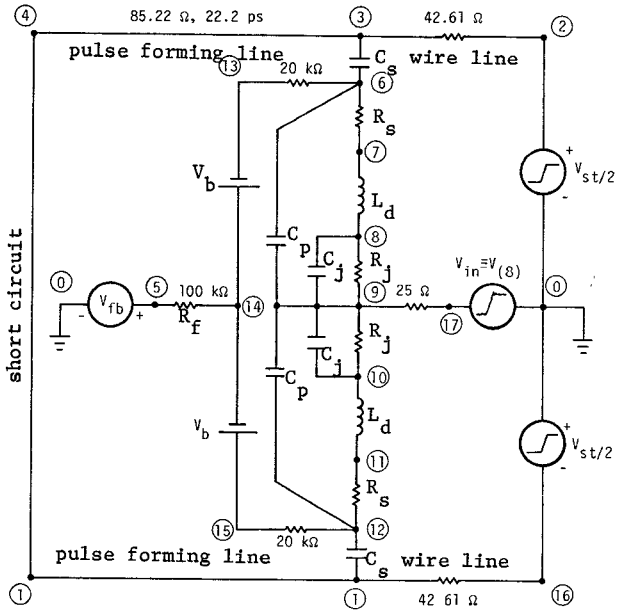


Figure 3. Sampling Diode Network With Strobe Pulse, Forming Line and Feed-Back Circuit (Node numbers on this diagram do not correspond to those in Figure 2)

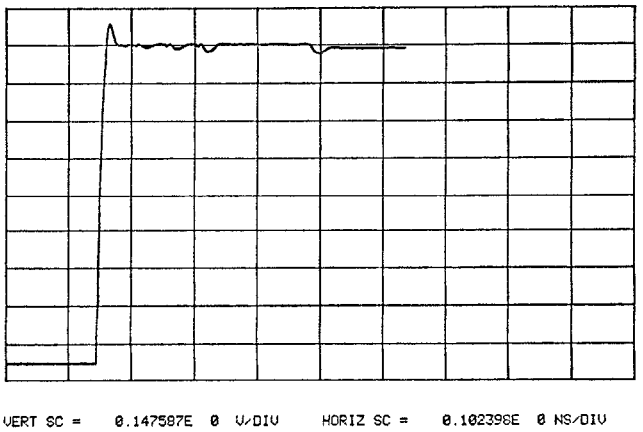


Figure 4. Structure Step Response V_8 of Fig. 2

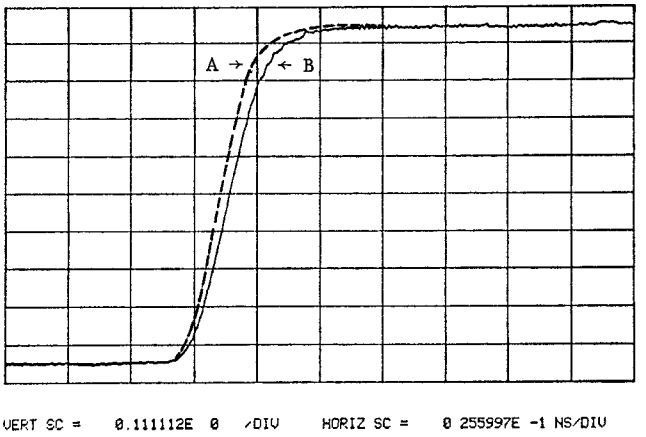


Figure 5. Simulated Sampling-Head Step Response vs. Bias Voltage.
(A: -1.76 volts, B: -1.63 volts).

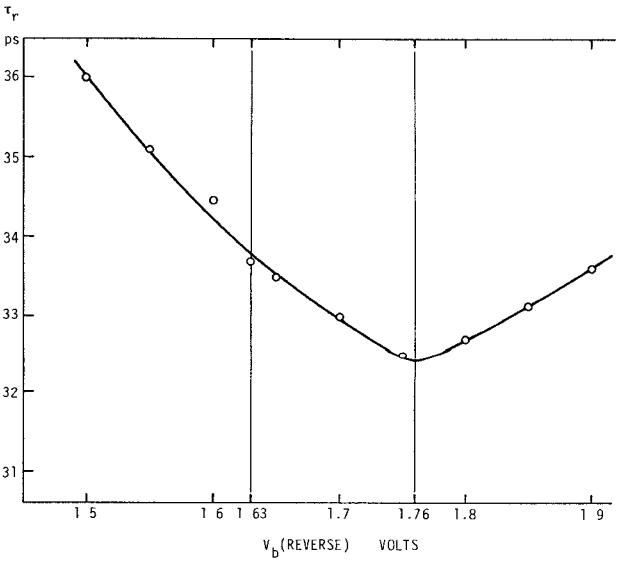


Figure 6. Displayed Transition Duration τ_r For a Tunnel Diode Transition Generator vs. Sampling Gate Bias V_b.